Sam Schiedermayer

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Summary

Low-power GPU hardware engineer with 4+ years developing pre+post silicon flows and infrastructure for taped out and shipped mobile, laptop, and automotive SoCs. Background spans firmware, silicon bring-up and measurement, RTL power analysis, and AI-assisted PPA tooling.

Experience

Senior GPU Hardware Engineer - Qualcomm (March 2023 - Present) - San Diego, CA

- Own and maintain the PPA feedback flow used by the entire GPU RTL design team (Synopsys RTL-Architect) on N3E, N2, and A14. Work directly with Synopsys Application Engineers to solve tool and flow challenges.
- Built and own a GPU power/performance projection flow in python that takes in per-rail measured data and computes second order power/performance based on DCVS/cdyn/leakage scaling data from synthesis. Used across multiple projects to left shift selection of synthesis knobs and DCVS plans, improving KPI FPS by >5%.
- Built AI based flow to take historical RTL+PPA diffs and suggest new RTL to improve PPA. Proven useful in improving congestion in the most congested hardmacro. Now working to target clock gating to save power.
- Built MCP server + set of skills for feeding agents PPA data from synthesis runs and analyzing the data in the manner that an engineer would. Enabled consistently similar results to prior manual analysis.
- Identify areas across the entire GPU that have poor clock gating, and flag high ROI registers to the RTL design team to reduce power consumption. Example: identified RTL in the cache that was wasting 2% of cache power.
- Run cross-functional meetings with RTL design highlighting problem points across all blocks for key PPA metrics. Resulted in fewer area surprises, timing issues, and clock gating issues in the X2 Elite Laptop GPU.

GPU Design Verification Intern - Apple (May 2022 - Aug 2022) - Austin, TX

- Developed a test plan to get an early performance comparison between 2 options for a shader core scheduler.
- Proved out early performance verification methodology to de-risk future design changes.

Autopilot Silicon Validation Co-op - Tesla (Jan 2021 - Aug 2021) - Palo Alto, CA

- Validated clock and power gating functionality across all IPs during bring-up of HW4 SoC.
- Conducted PVT characterization during bring-up of multiple IPs. Produced schmoo plots and similar data.
- Developed and validated Linux+firmware patches to enable new intermediate DCVS states for NPU.
- Wrote C, C++, and OpenCL programs to create power virus workloads for multiple IPs.

Undergraduate Teaching+Research Assistant - University of Wisconsin, Madison (Spring+Fall 2022) - Madison, WI

- Held office hours and graded papers for ECE555 - Digital Circuits and Components.
- Taught students how to use Cadence Virtuoso for schematic capture and layout with ASAP7 7nm PDK.

Software Engineering Intern - Miller Electric Mfg. (Summer 2020) - Appleton, WI

- Wrote software modules in embedded C++ for timers and GPIO on ST microcontrollers, including tests.

Software Engineering Intern - Liveality Inc. (Part time June 2018 - Aug 2019) - Greenville, WI

- Worked start to finish on a native iOS and Android app, maintained EAA AirVenture event app, and created computer vision solutions using OpenCV and TensorFlow for tail number detection + defect detection.

Education

University of Wisconsin - Madison (GPA: 3.75/4.0)

B.S. Electrical Engineering, Computer Science (Dec 2022)

- Graduated at an accelerated rate in only 6 semesters, while taking graduate level courses.
- ASIC Design - Created a robot control ASIC including RTL, testbenches, and synthesizing to Cyclone IV FPGA.
- Digital Circuits - Designed a basic NN accelerator, from microarchitecture to manual layout in Cadence Virtuoso.

Skills

SystemVerilog, Bash/Csh, Python, C, C++, Oscilloscope, Synopsys Tools (RTL-Architect, PTPX, Fusion Compiler), Computer Architecture, VLSI, GPU Architecture, Linux, Power Modeling, DVFS/DCVS, Power Architecture